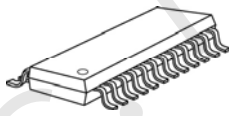
16-Channel PWM Constant Current LED Driver for 1:8 Time-Multiplexing Applications

Features

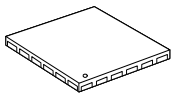
- 3.0V-5.5V supply voltage
- 16 constant current output channels
- Constant output current range:
  - 2 ~ 45mA @ 5V supply voltage
  - 2 ~ 30mA @ 3.3V supply voltage
- Excellent output current accuracy:
  Between channels: < ±2.5%(Max.)
  Between ICs: < ±3%(Max.)
- Built-in 4K-bit SRAM to support time-multiplexing for 1 ~ 8 scans
- 16/15/14/13-bit color depth PWM control to improve visual refresh rate
- 6-bit current gain，12.5% ~ 100%
- LED failure isolation
  - LED failure induced cross elimination
- LED open detection
- Integrating ghost elimination circuit
- Intelligent power saving modes
  - Dynamic power saving (when all frame data is zero)
  - Dynamic+ power saving (when displaying dynamic video with various brightness)
- GCLK multiplier technology
- Maximum DCLK frequency: 30MHz

Shrink SOP



GP: SSOP24L-150-0.64

QFN



GFN: QFN24L-4x4-0.5

Product Description

MBI5251 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16/15/14/13-bit grayscale resolution. With Macroblock's proprietary S-PWM technology, it is able to reduce the flickers and improves the image fidelity. MBI5251 features a 16-bit shift register which converts serial input data into each pixel's grayscale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:8 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5251 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

Through compulsory error detection, MBI5251 detects individual LED for open-circuit errors without extra components. MBI5251 is equipped with an innovative cross elimination function, as it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination circuit eases the ghost problems.

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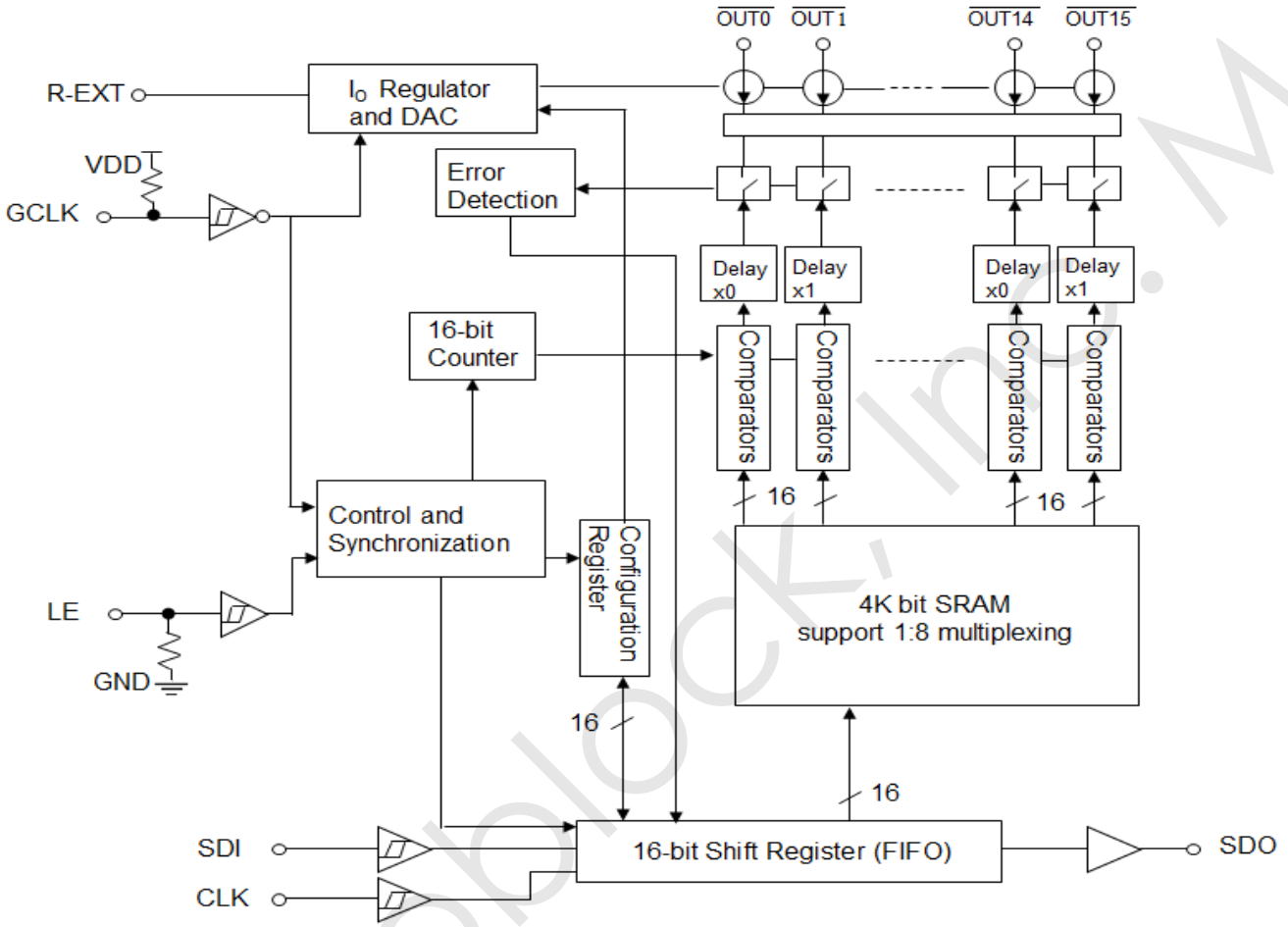
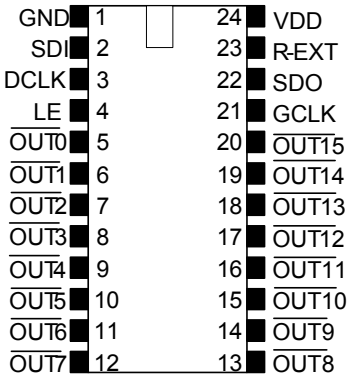
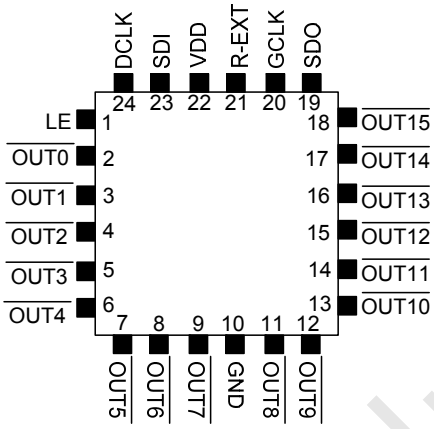
Block Diagram



Pin Configuration



MBI5251 GP



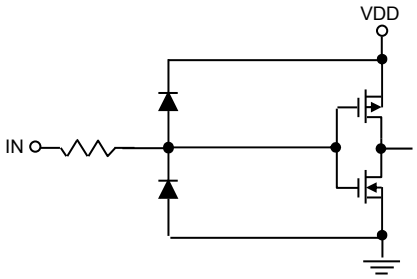
MBI5251GFN

Terminal Description

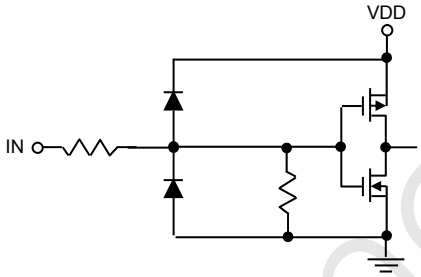
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Grayscale clock terminal Clock input for grayscale. The grayscale display is counted by grayscale clock compared with input data.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

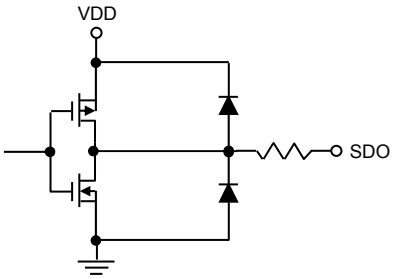
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~5.5	V
Input Pin Voltage (SDI, DCLK, GCLK, LE)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Ports		V_{DS}	-0.5~7	V
Output Current		I_{OUT}	+45	mA
GND Terminal Current		I_{GND}	735	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP Type	P_D	1.47	W
	GFN Type		3.37	
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GP Type	$R_{th(j-a)}$	85	°C/W
	GFN Type		37	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883H Method 3015.8)	HBM	Class 3A (7KV)	-
	Machine Mode (ANSI/ ESD S5.2-2009)	MM	Class M4 (≥400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

**Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	7.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=5.4V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=2mA V_{DS}=1.0V	R_{ext}=7.2KΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=2mA V_{DS}=1.0V	R_{ext}=7.2KΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		-	450	-	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK =0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.8	-	mA
		I_{DD}(off) 2	R_{ext}=7.2KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5	-	
		I_{DD}(off) 3	R_{ext}=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	12	-	
	"On" (GCLK=20MHz)	I_{DD}(on) 2	R_{ext}=7.2KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	5.5	-	
		I_{DD}(on) 3	R_{ext}=320Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	13	-	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	7.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=3.7V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=7.2KΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=7.2KΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		-	450	-	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK=0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.8	-	mA
		I_{DD}(off) 2	R_{ext}=7.2KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4	-	
		I_{DD}(off) 3	R_{ext}=320Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	10.5	-	
	"On" (GCLK=20MHz)	I_{DD}(on) 2	R_{ext}=7.2KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	4.5	-	
		I_{DD}(on) 3	R_{ext}=320Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	11.5	-	

*One channel on.

Test Circuit for Electrical Characteristics

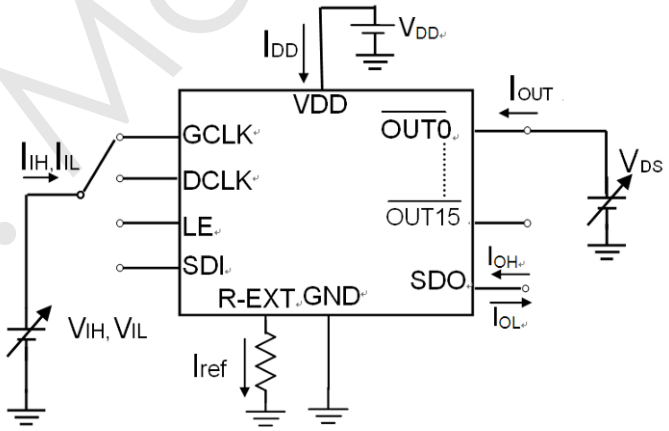


Figure 2

Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	5	-	-	ns
	LE ↑ - DCLK ↑	t_{SU1}		8	-	-	ns
	LE ↓ (Vsync) - GCLK	t_{SU2}		1200	-	-	ns
	LE ↓ - DCLK ↑	t_{SU3} **		50	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		6	-	-	ns
	DCLK ↑ - LE	t_{H1}		8	-	-	ns
	GCLK - LE ↑ (Vsync)	t_{H2}		300	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	22	25	ns
	GCLK - $\overline{OUT2n}$*	t_{PD1}		-	35	-	ns
	LE - SDO	t_{PD2}**		-	30	40	ns
Pulse Width	LE	$t_{w(LE)}$		15	-	-	ns
Command to Command		Tcc		50	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Grayscale Clock Frequency***		F_{GCLK}		-	-	33	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}		-	-	16.6	MHz
Min Clock(GCLK/ DCLK) Pulse Width***		$t_{W(CLK)}$		12	-	-	ns
Ratio of (GCLK freq)/ (DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory Error Detection Operation time****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	15	20	ns
Output Fall Time of Output Ports		t_{OF}		-	15	20	ns
Output Rise Time of Output Ports (Slow)		t_{OR}		-	30	40	ns
Output Fall Time of Output Ports (Slow)		t_{OF}		-	30	40	ns
Dead Time positive level		t_{dth}		300	-	-	ns
Dead Time negative level		t_{dtl}		1200	-	-	ns

* Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

** In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

*** The Grayscale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

**** It is recommended to use longer duration than the minimum error detection time.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE - DCLK ↑	t_{SU1}		10	-	-	ns
	LE ↓ (Vsync) - GCLK	t_{SU2}		1200	-	-	ns
	LE ↓ - DCLK ↑	t_{SU3} **		52	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		8	-	-	ns
	DCLK ↑ - LE	t_{H1}		10	-	-	ns
	GCLK - LE ↓ (Vsync)	t_{H2}		300	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	25		ns
	GCLK - $\overline{OUT2n}$*	t_{PD1}		-	45	-	ns
	LE - SDO	t_{PD2}**		-	40	-	ns
Pulse Width	LE	$t_{W(LE)}$		16	-	-	ns
Command to Command		tcc		52	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Grayscale Clock Frequency***		F_{GCLK}		-	-	20	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}		-	-	10	MHz
Min Clock(GCLK/ DCLK) Pulse Width****		$t_{W(CLK)}$		13	-	-	ns
Ratio of (GCLK freq)/ (DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory Error Detection Operation time*****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	25	35	ns
Output Fall Time of Output Ports		t_{OF}		-	25	35	ns
Dead Time positive level		tdth		300	-	-	ns
Dead Time negative level		tdtl		1200	-	-	ns

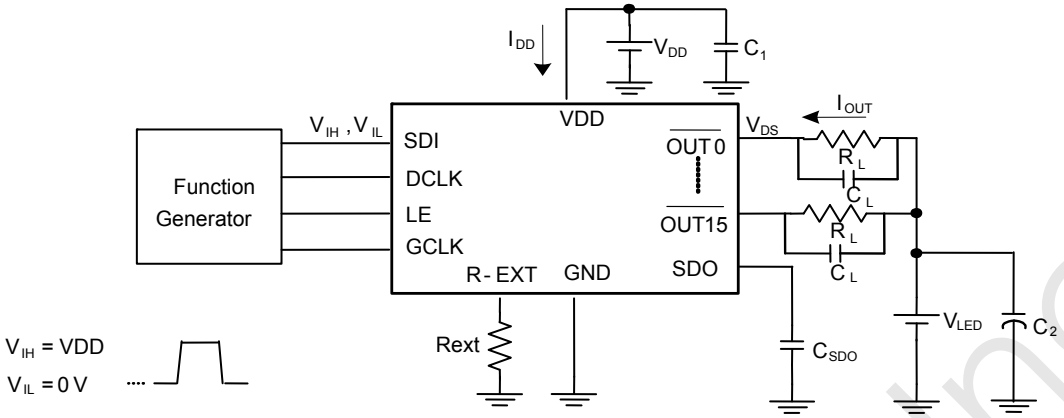
* Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

** In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

*** The Grayscale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

**** It is recommended to use longer duration than the minimum error detection time.

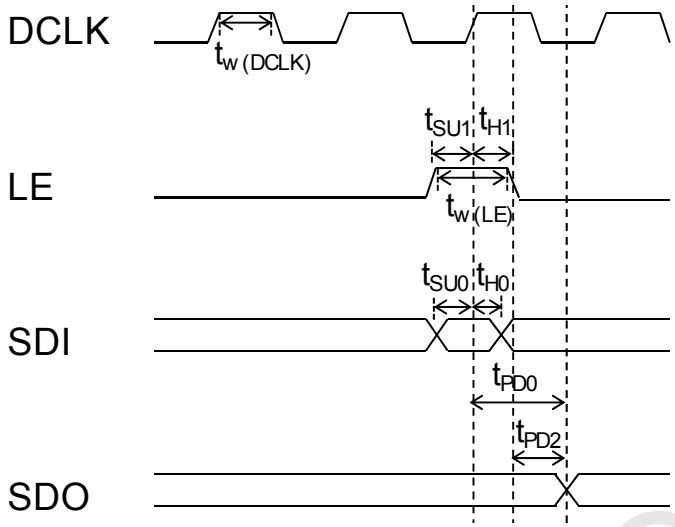
Test Circuit for Switching Characteristics



Timing Waveform

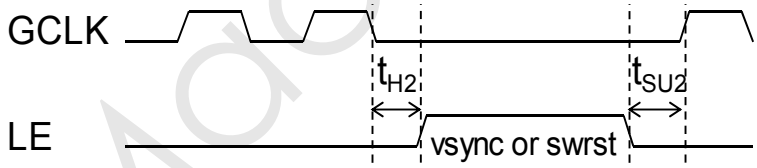
Control timing

(1)

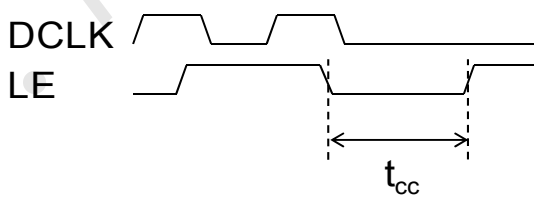


(2)

(3)



(4)



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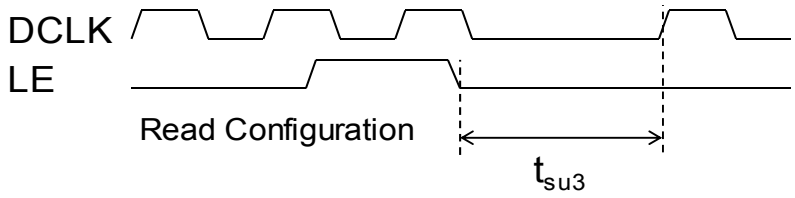
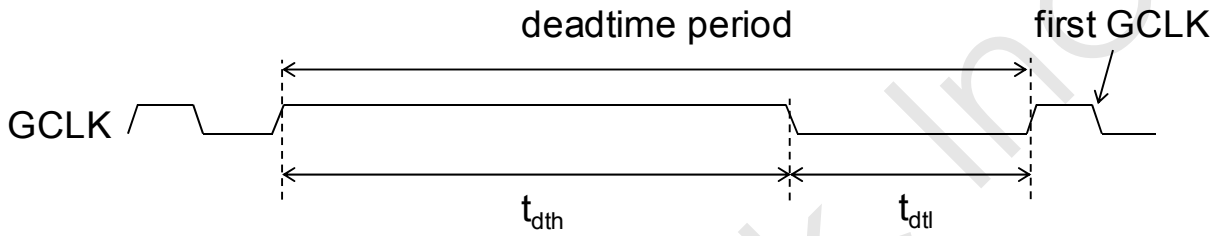
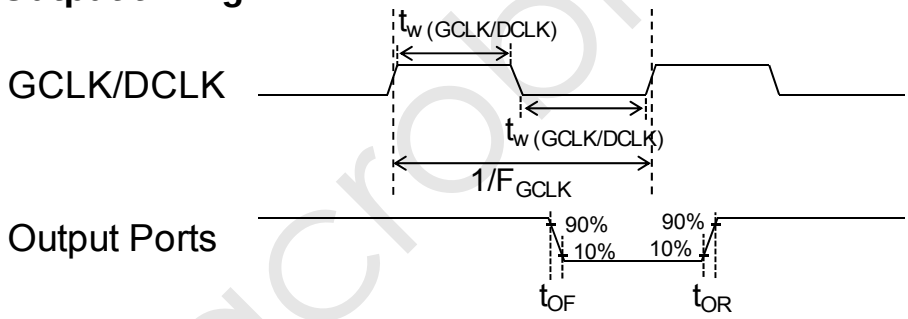


(6)



Output timing



Control Command

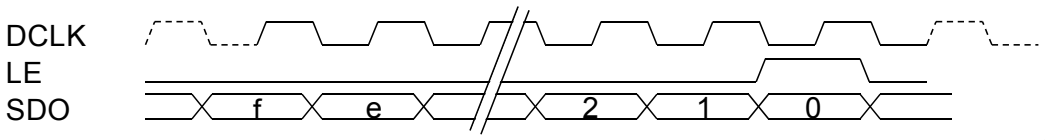
Command Name	Signals Combination		Description
	LE	Number of DCLK Rising Edge when LE is asserted	Action of Command
Stop Compulsory Error detection	High	1	Stop compulsory LED open detection
Data Latch	High	1	Serial data are transferred to the input data buffers.
VSYNC	High	2	Vertical Synchronal signal. Displaying frame will be updated to output channel
Write Configuration 1*	High	4	Serial data are written to the configuration register 1
Read Configuration 1	High	5	Serial data are read from the configuration register 1
Start Compulsory Error detection	High	7	Start compulsory LED open detection
Write Configuration 2*	High	8	Serial data are written to the configuration register 2
Read Configuration 2	High	9	Serial data are read from the configuration register 2
Software Reset	High	10	Reset the behavior of MBI5251 except the value of configuration registers.
Write Configuration 5*	High	13	Serial data are written to the configuration register 5
Pre-Active	High	14	Pre-Active command needs to be sent before “Write Configuration” command
Read Configuration 5	High	21	Serial data are read from the configuration register 5

*Those commands can only be activated after “Confirm command”; otherwise, they will be invalid.
Note: When the power is on, Vsync command will be valid only after 16 times of “Data Latch” commands that have been sent in advance.

Waveform of Commands

The following figures show the waveforms of commands.

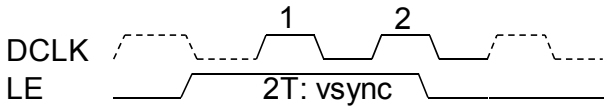
Data Latch



Note: GCLK can not stop during this command, and GCLK_freq / DCLK_freq >= 1/5

Data Latch command is used to latch the 16-bit shift register from SDI to internal SRAM buffer. When this command is received, the last 16 bits data before the falling edge of LE will be latched into SRAM, as shown in the above waveform, and MSB bit needs to be sent first.

Vertical Sync (VSYNC)

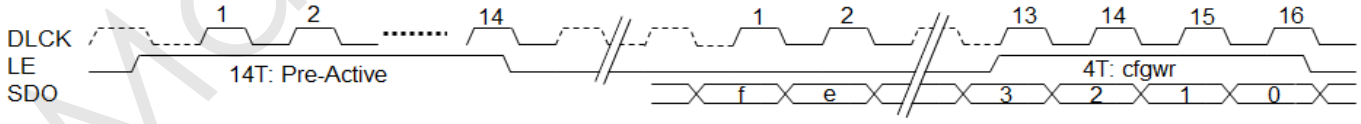


"VSYNC" command is used to update frame data on output channels ($\overline{OUT0}$ ~ $\overline{OUT15}$). There are some timing limitations between signal "LE" and "GCLK"; and please refer to the section of "Vsync Command Operation" for details.

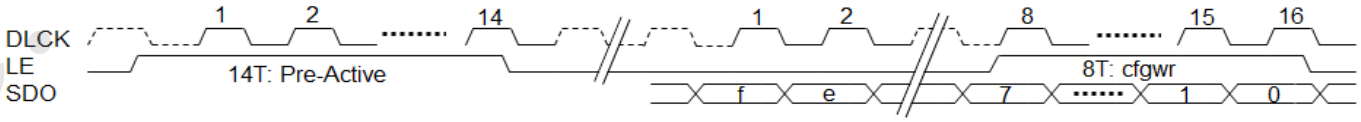
Write Configuration

Write configuration (cfgwr) command is used to program the configuration register of MBI5251. The "Pre-Active" command must be sent in advance. When this command is received, the last 16 bits data before the falling edge of LE will be latched into configuration register, as shown in the below waveforms, and MSB bit needs to be sent first.

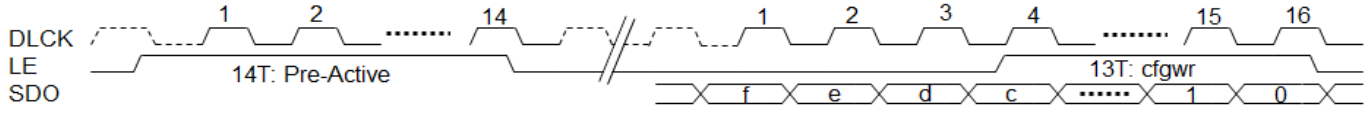
Write Configuration 1



Write Configuration 2



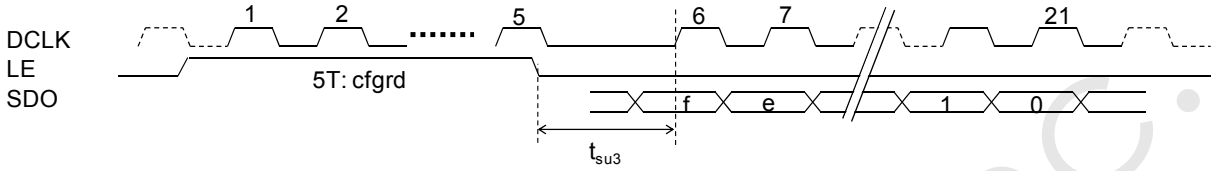
Write Configuration 5



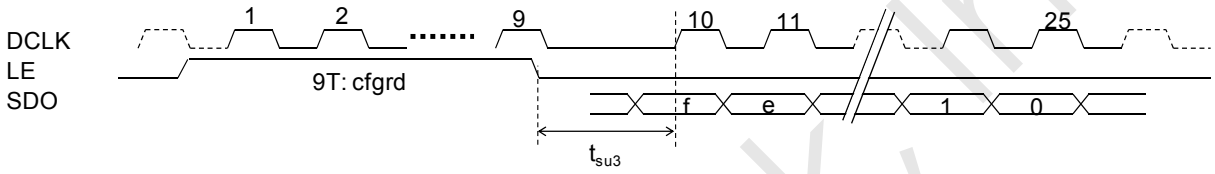
Read Configuration

Read configuration (cfgrd) command is used to read the configuration register of MBI5251. When this command is received, the 16-bit data of configuration register will be shifted out from SDO pin, as shown in the below waveforms, and MSB bit will be shifted out first.

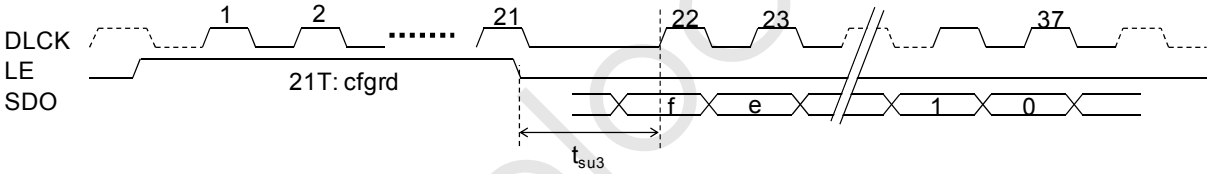
Read Configuration 1



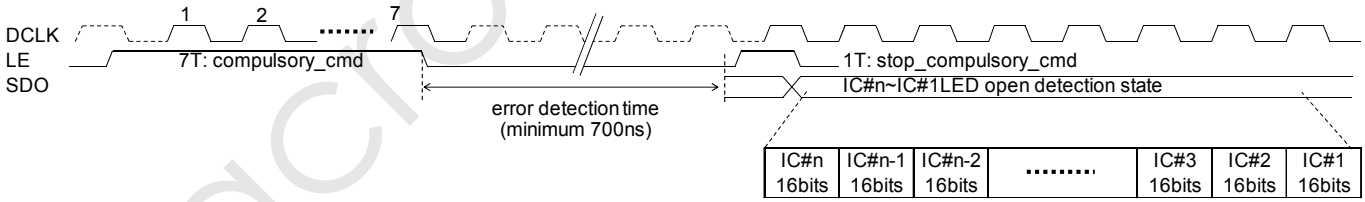
Read Configuration 2



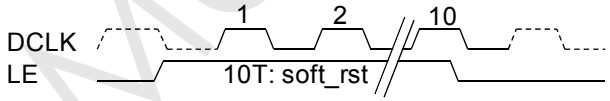
Read Configuration 5



Compulsory error detection



Software Reset



Software reset command makes MBI5251 go back to the initial state except configuration register value. After this command is received, the output channels will be turned off and will display again with last grayscale value after new “Vsync” command is received.

Definition of Configuration Register 1

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
F	Read/Write	Reserved	0 (Default)	Reserved
E	Read/Write	PWM counting mode	0 (Default)	PWM is forward counting
			1	PWM is backward counting
D	Read/Write	LED failure induced cross elimination	0 (Default)	Disable
			1	Enable
C~B	Read/Write	Reserved	00 (Default)	Reserved
A~8	Read/Write	Number of scan lines	000 001 010 011 (Default) ~ 111	000: 1 lines 001: 2 lines 010: 3 lines 011: 4 lines (Default) 100: 5 lines 101: 6 lines 110: 7 lines 111: 8 lines
7~6	Read/Write	S-PWM mode	00 (Default)	The 65536 GCLK (16-bit) PWM cycle is divided into 64 sections, each section has 1024 GCLK.
			01	The 32768 GCLK (15-bit) PWM cycle is divided into 32 sections, each section has 1024 GCLK. User still sends 16bit data with 1 bit 0 in LSB bits. Ex., {15'h1234, 1'h0}.
			10	The 16384 GCLK (14-bit) PWM cycle is divided into 32 sections, each section has 512 GCLK. User still sends 16bit data with 2 bit 0 in LSB bits. Ex., {14'h1234, 2'h0}.
			11	The 8192 GCLK (13-bit) PWM cycle is divided into 16 sections, each section has 512 GCLK. User still sends 16bit data with 3 bit 0 in LSB bits. Ex., {13'h1234, 3'h0}.
5~0	Read/Write	Current Gain	000,000 ~ 111,111	[000,000] 12.5% ~ [111,111] 100%

Default setting of configuration register is 16'h033f

Definition of Configuration Register 2

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
15	Read/Write	Reserved	0 (Default)	Reserved
			1	
14	Read/Write	Reserved	0 (Default)	Reserved
			1	
13~11	Read/Write	Reserved	000 (Default)	Reserved
10	Read/Write	Double refresh	0 (Default)	Disable
			1	Enable
9	Read/Write	GCLK multiplier	0 (Default)	Disable
			1	Enable
8~5	Read/Write	Reserved	0000 (Default)	Reserved
4~0	Read/Write	Reserved	00000 (Default)	Reserved

Default setting of configuration register is 16'h0000

Definition of Configuration Register 5

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
15~8	Read/Write	Reserved	00000001 (Default)	Reserved
7~5	Read/Write	Open Error detection voltage threshold	000 (Default)	[000] level 0 ~ [111] level 7
4~0	Read/Write	Lower ghost elimination	11111 (Default)	[00000] level 0 ~ [11111] level 7

Default setting of configuration register is 16'h011f

Number of Scan Line

MBI5251 supports 1 to 8 scan lines. Please set the Configuration Register 1, bit [10:8] according to the application. The default value '011' is 4 scan lines.

Grayscale Mode and Scan-type S-PWM

MBI5251 provides a selectable 16/15/14/13-bit grayscale by setting the Configuration Register 1, bit [7:6]. The default value is set to '00' for 16-bit color depth. In 15/14/13-bit grayscale modes, users should still send 16-bit data with 1/2/3-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

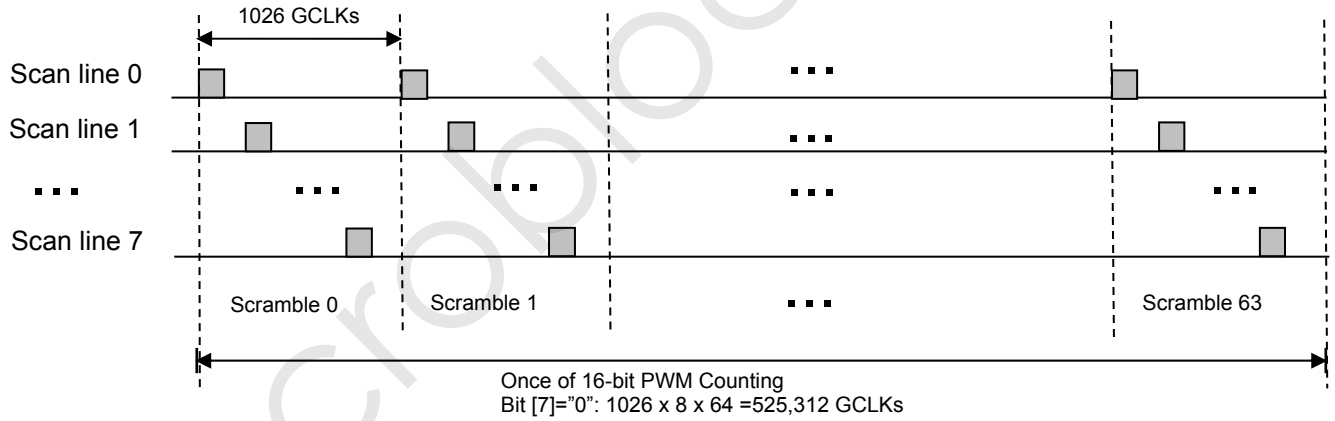
MBI5251 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be separated into MSB (Most Significant Bits) and LSB (Least Significant Bits) of grayscale cycles. The MSB information can be divided into many refresh cycles to achieve overall same high bit resolution.

GCLK Multiplier

MBI5251 provides a GCLK multiplier function by setting the Configuration Register 2, bit [9]. The default value is set to '0' for GCLK multiplier disable.

GCLK multiplier disabled (Configuration Register 2, bit [9] = 0)

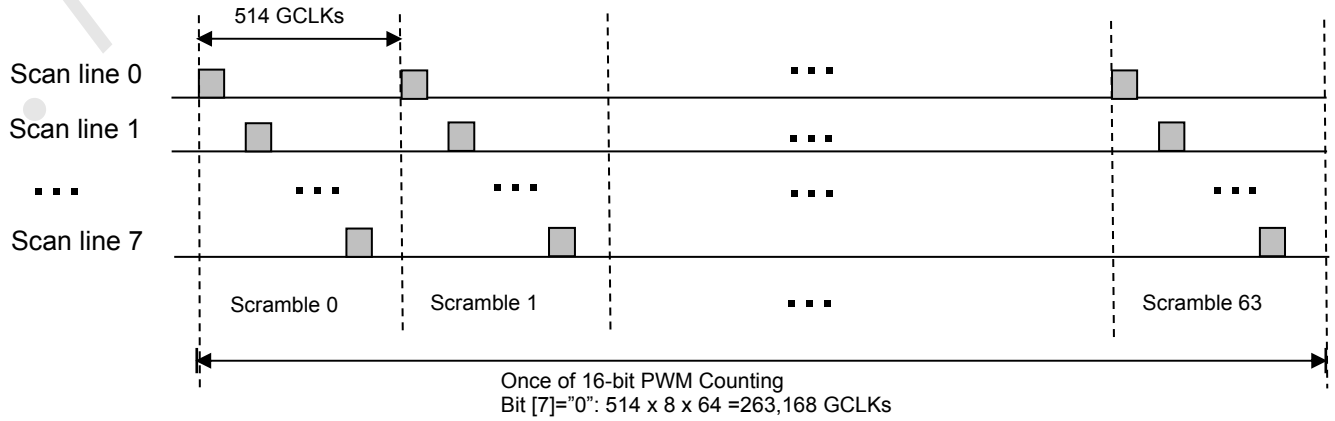
Display sequence of 64 scrambles



: Output ports are turned "on".

GCLK multiplier enabled (Configuration Register 2, bit [9] = 1)

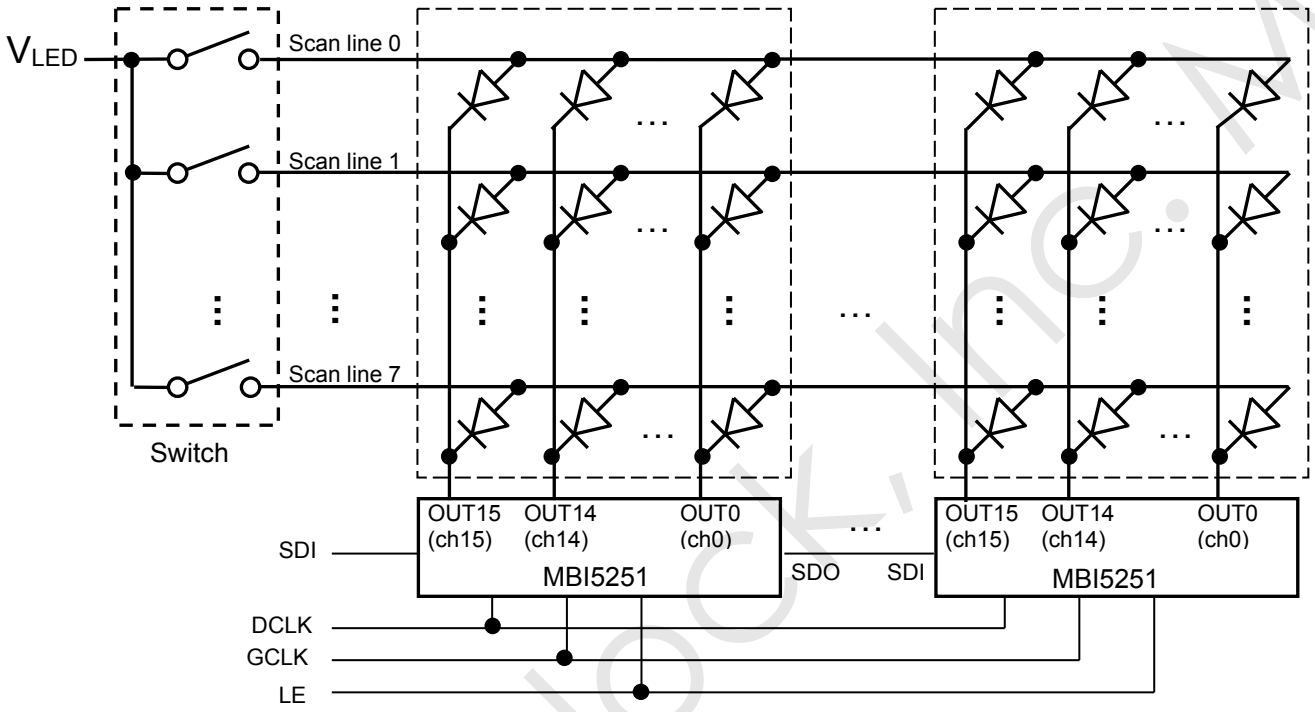
Display sequence of 64 scrambles



: Output ports are turned "on".

Operation Principles

Scan type application structure



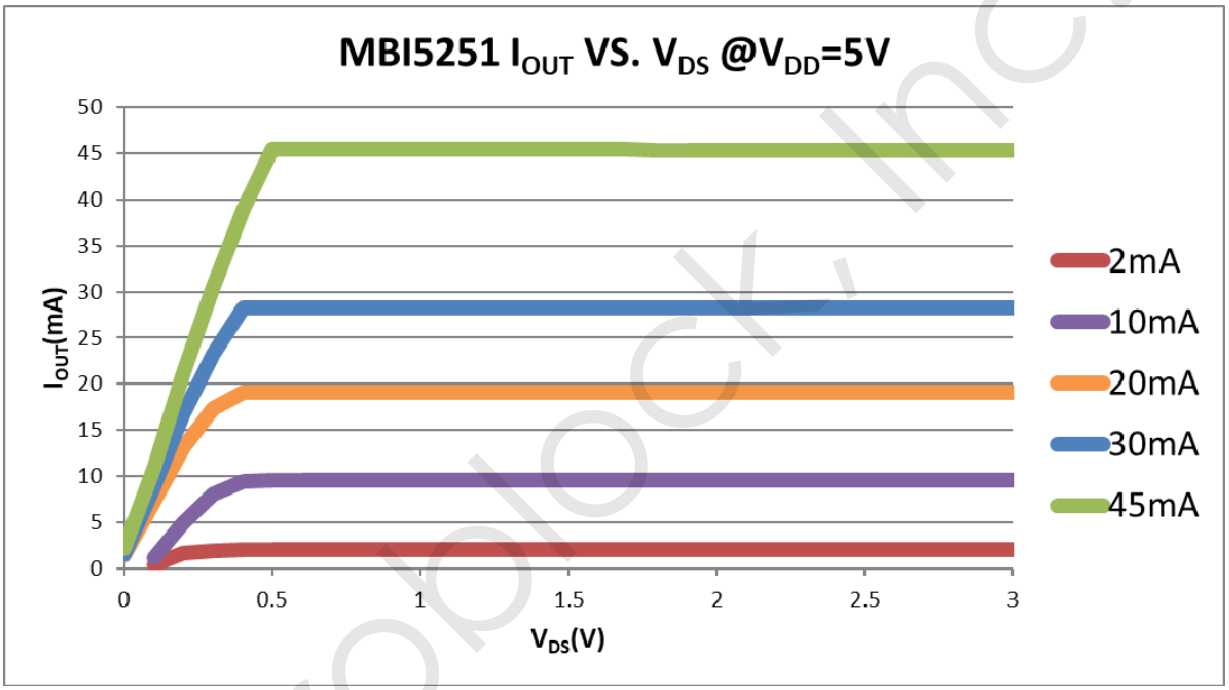
The above figure shows the suggested application structure of scan type scheme with 8 scan lines. The grayscale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 16 channels ($\overline{OUT0}$ ~ $\overline{OUT15}$) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage is described in the application note.

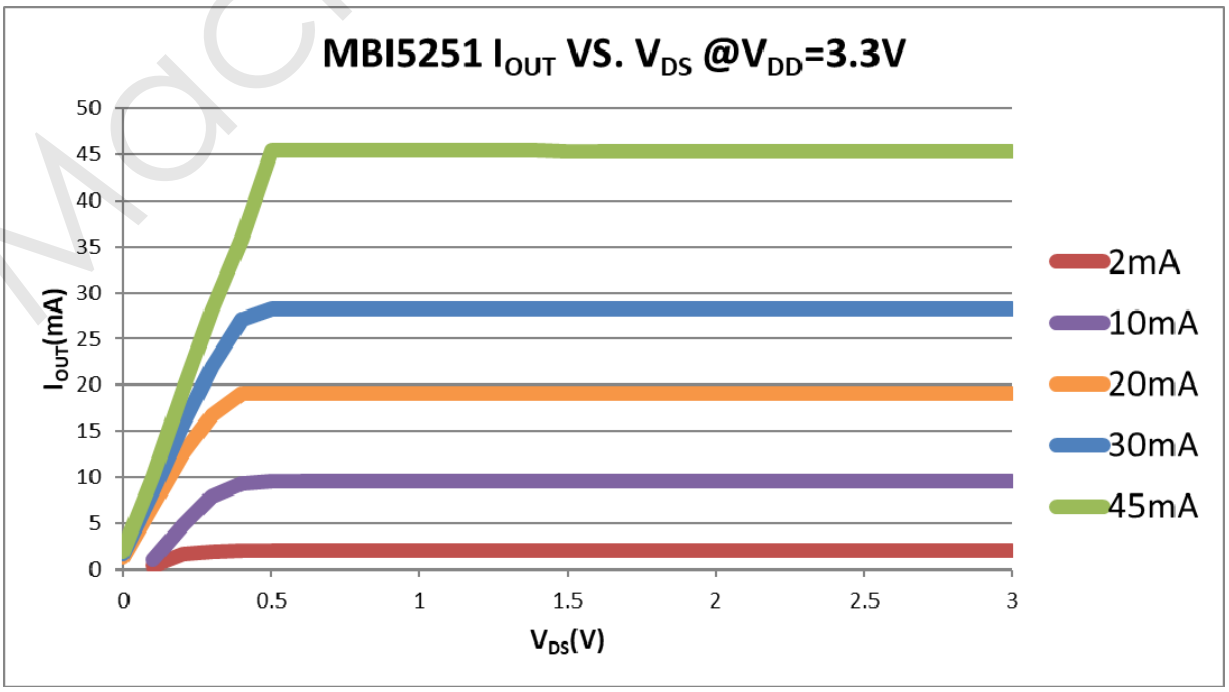
Constant Current

In LED display application, MBI5251 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximuml current variation between channels is less than 2.5%, and that between ICs is less than ±3%

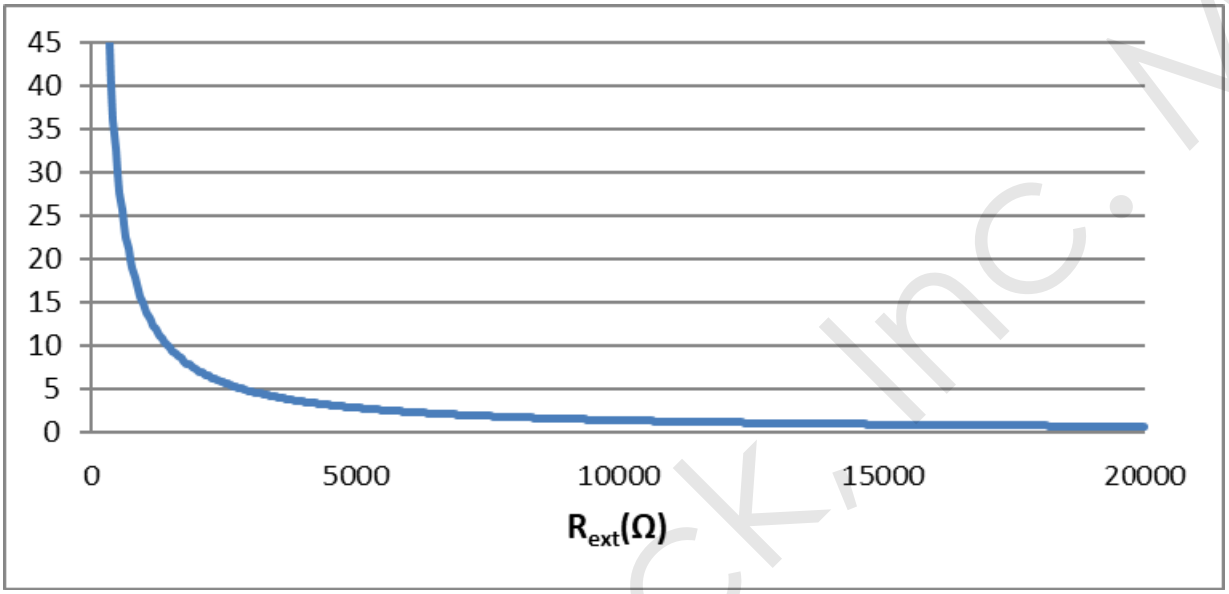
2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.



Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$ = 0.61Volt

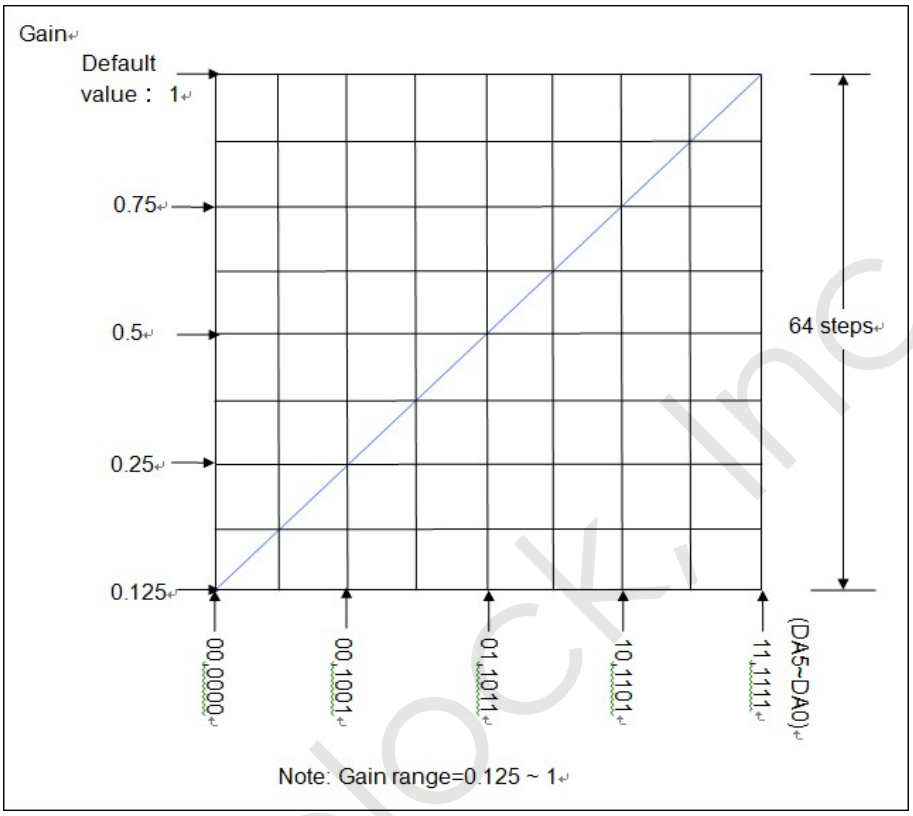
I_{OUT} = ($V_{R\text{-}EXT}$ / R_{ext}) x G x 24

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit5 to bit0 of the configuration register. The recommended value of G is 0.5

For your information, the output current is about 20mA when Rext = 700Ω if G is set to 1

The formula and setting for G are described in the next section.

Current Gain Adjustment



The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number, i.e., ranging from 6'b000000 to 6'b111111, these bits allow user to set the output current gain up to 64 levels. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	DA5	DA4	DA3	DA2	DA1	DA0

Bit 5 to bit 0 are DA5 ~ DA0.
The relationship between these bits and current gain G is:

$G = 0.125 + (D / 63) \times 0.875$

D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D = DA5 \times 2^5 + DA4 \times 2^4 + DA3 \times 2^3 + DA2 \times 2^2 + DA1 \times 2^1 + DA0 \times 2^0$

In other words, these bits can be looked as 6-bit mantissa DA5~DA0

For example:

G = 0.5
D = (0.5 - 0.125) / 0.875 x 63 = 27
D in binary form would be:
D = 27
$= 0 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b011011

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is:

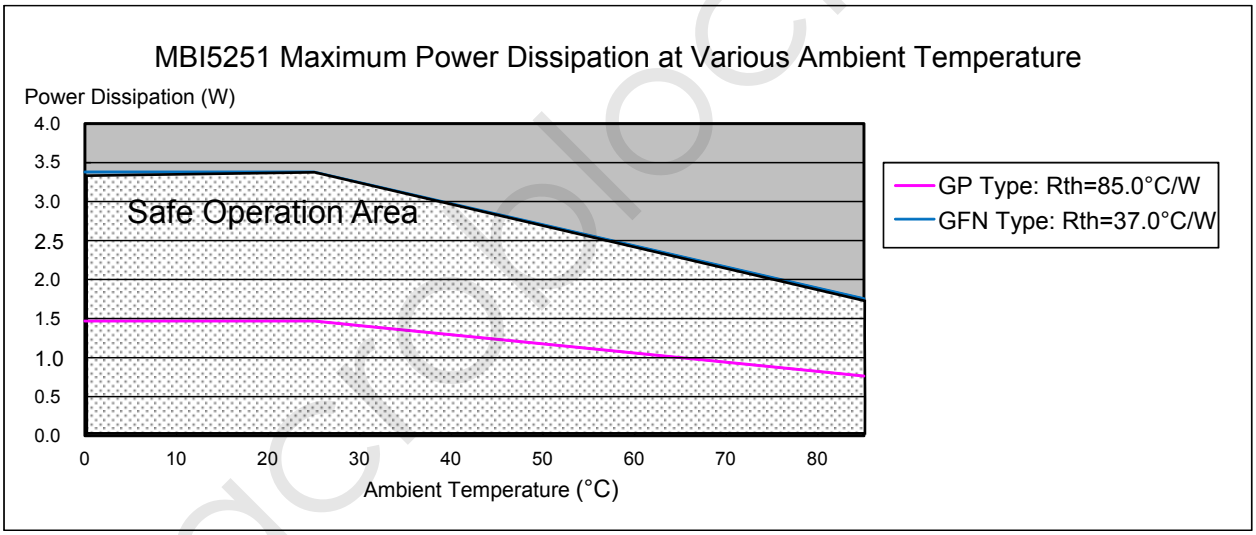
$P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$. Therefore, to keep $P_D(act) \leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT} = \{[(Tj–Ta) / R_{th(j-a)}] – (I_{DD} \times V_{DD})\} / V_{DS} / Duty / 16$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	85	1.47
GFN	37	3.37

The maximum power dissipation, $P_D(max)=(Tj – Ta) / R_{th(j-a)}$, decreases as the ambient temperature increases.

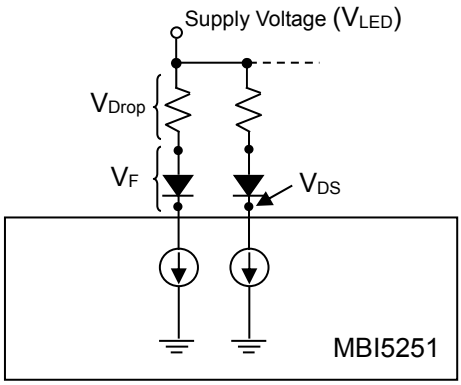


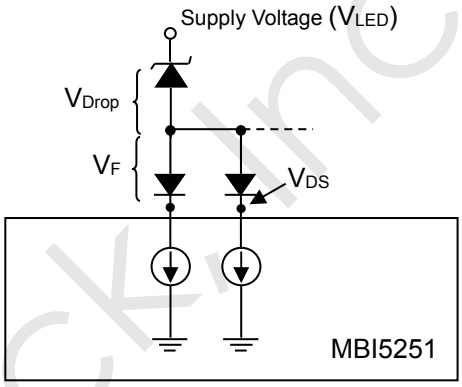
LED Supply Voltage (V_{LED})

MBI5251 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT} = 2 ~ 45mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED} = 5V and $V_{DS}=V_{LED} – V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS} = (V_{LED} – V_F) – V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.





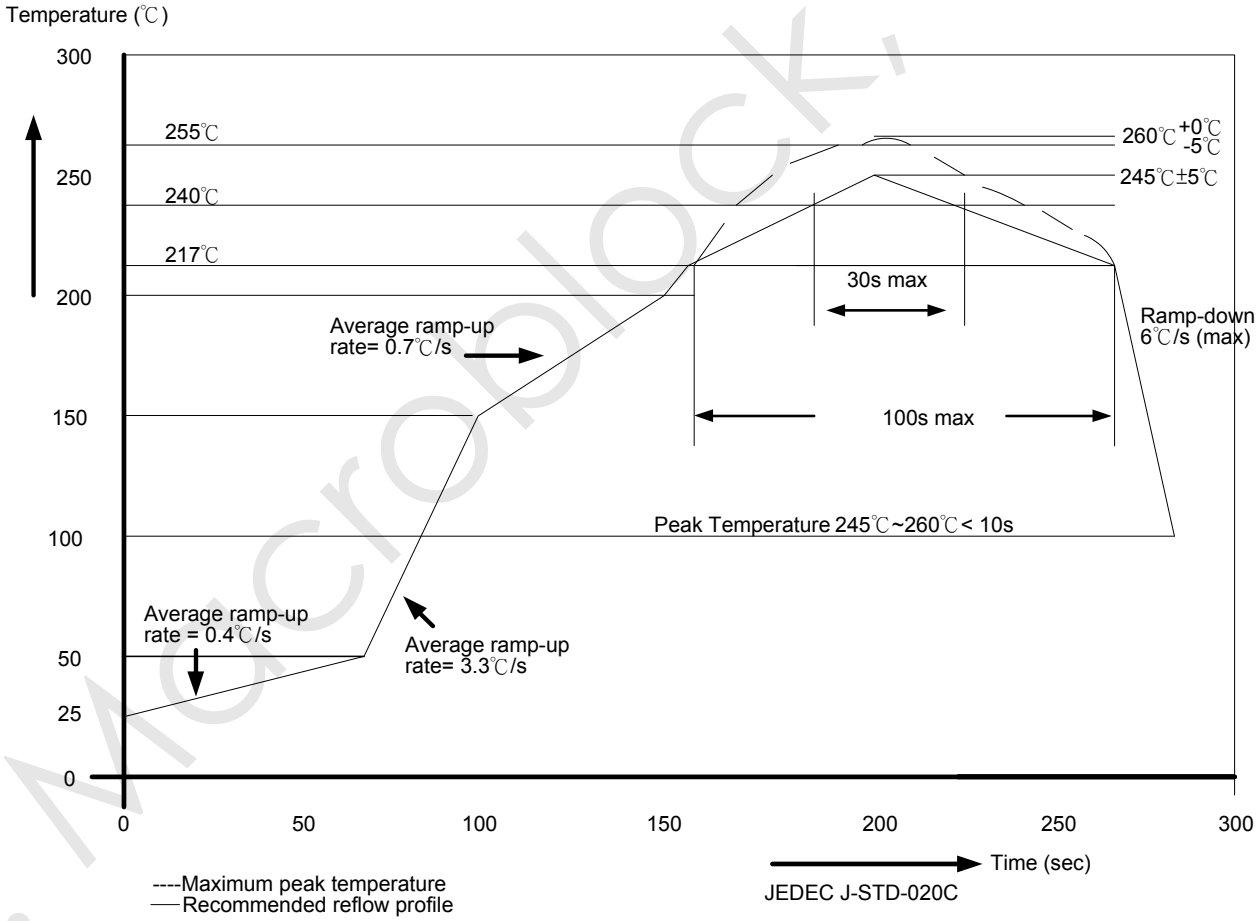
Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245℃ to 260℃ for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

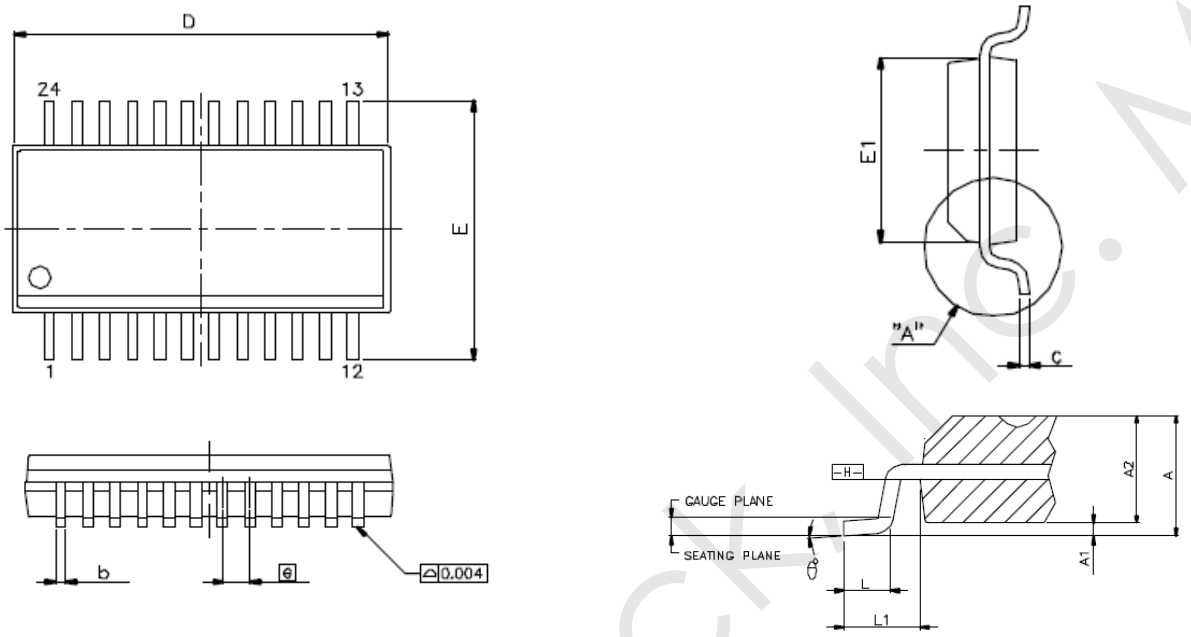
For managing MSL3 Package, it should refer to JEDEC J-STD-020C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

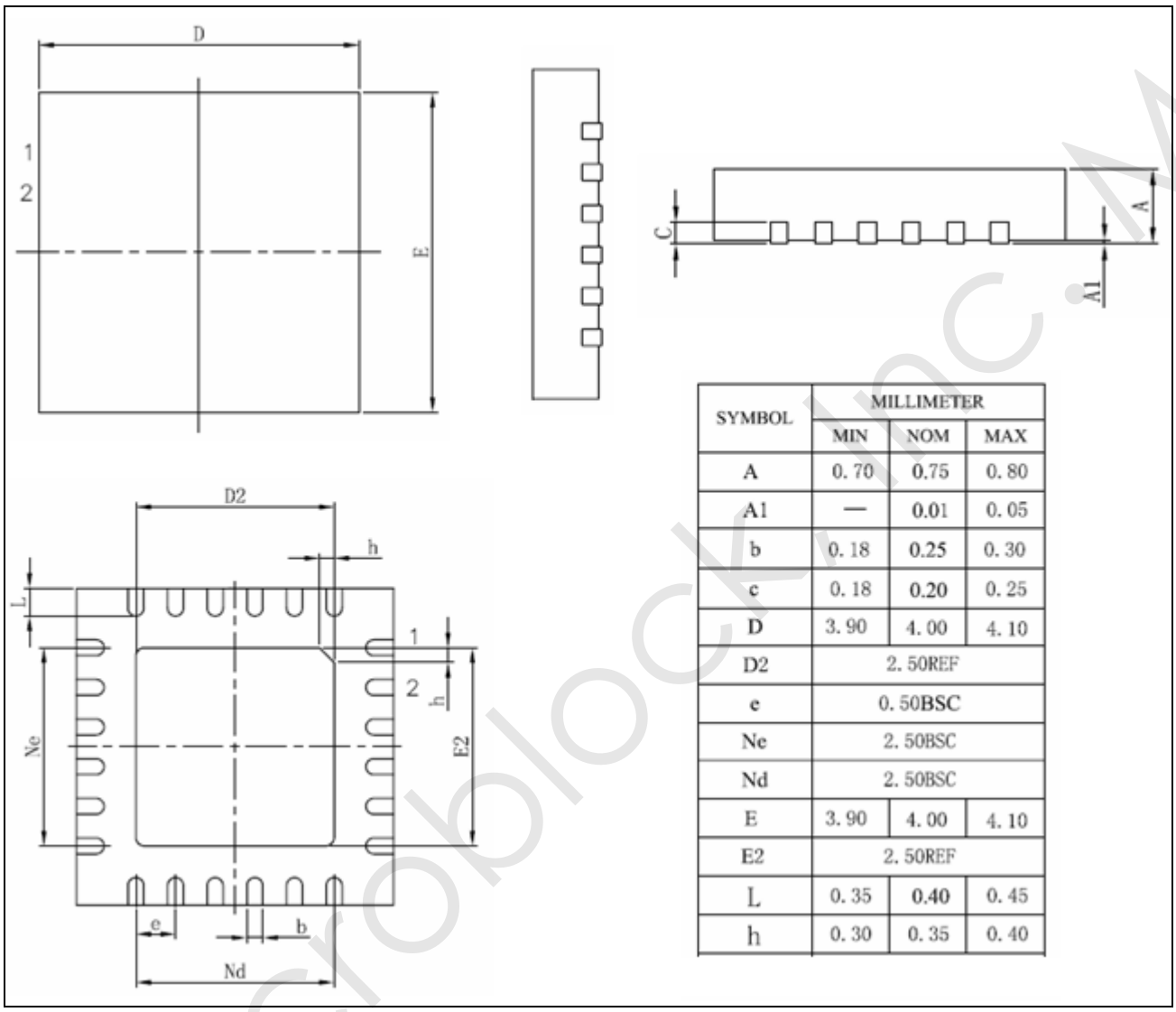
*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
Θ°	0	—	8	0	—	8

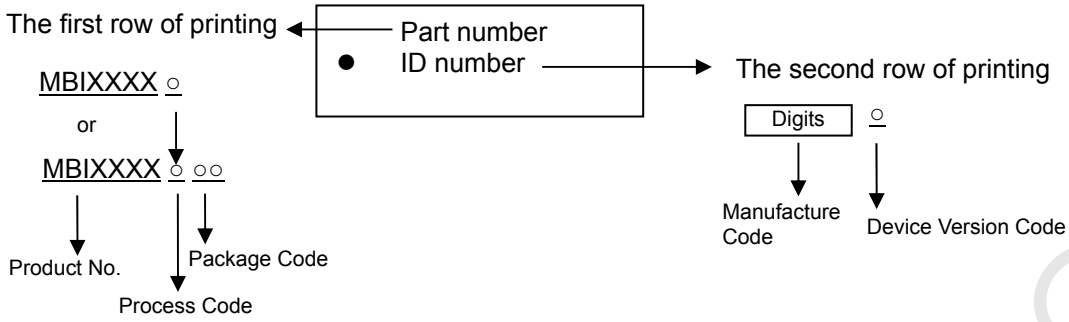
MBI5251GP Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MBI5251GFN Outline Drawing

Product Top Mark Information



Product Revision History

Preliminary Datasheet Version	Device Version Code
V1.00	A
V1.01	A

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5251GP-A	SSOP24L-150-0.64	0.11
MBI5251GFN-A	QFN24L-4*4-0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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